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Claims

[c1] A method of defining spacings between the gates of field effect transistors (FETs) of an integrated circuit and the source and drain regions thereof, the spacings differing in width between a first FET and a second FET, comprising:
forming gate stacks of said integrated circuit over a substrate;
forming first spacers on sidewalls of said gate stacks;
forming second spacers over said first spacers;
forming source and drain regions of said first FET in alignment with said second spacers of a first gate stack of said gate stacks;
removing said second spacers;
anisotropically etching said first spacers of a second gate stack of said gate stacks in a substantially vertical direction to remove horizontally extending portions of said first spacers; and
forming source and drain regions of said second FET in alignment with portions of said first spacers of said first gate stack which remain after said etching.

[c2] The method according to claim 1 wherein said first FET

is an n-type FET (NFET) and said second FET is a p-type FET (PFET).

[c3] The method according to claim 2 wherein said gate stacks of said first and second FETs are aligned end-to-end in a horizontal direction over said substrate.

[c4] The method according to claim 1 wherein said substrate is a silicon-on-insulator substrate having an upper layer including a single-crystal semiconductor.

[c5] The method according to claim 4 wherein said single-crystal semiconductor consists essentially of silicon.

[c6] The method according to claim 2 further comprising forming a self-aligned silicide aligned to said source and drain regions of said NFET and said PFET.

[c7] The method according to claim 6 further comprising forming source and drain extensions of said NFET aligned to said gate stack of said NFET.

[c8] The method according to claim 7 further comprising forming a thin dielectric on said gate stack of at least said PFET and forming source and drain extensions of said PFET aligned to said thin dielectric.

[c9] The method according to claim 8 wherein said thin dielectric is formed by local thermal oxidation.

[c10] The method according to claim 2 wherein said etching is performed by a process including a reactive ion etch.

[c11] The method according to claim 10 wherein said first spacers consist essentially of silicon nitride and said second spacers consist essentially of silicon dioxide.

[c12] The method according to claim 10 wherein said first spacers consist essentially of silicon dioxide and said second spacers consist essentially of silicon nitride.

[c13] The method according to claim 6 wherein said silicide is a silicide of cobalt.

[c14] The method according to claim 13 further comprising forming a self-aligned silicide aligned to said gate stacks of said NFET and said PFET.

[c15] A method of defining spacings between the gates of field effect transistors (FETs) of an integrated circuit and the source and drain regions thereof, the spacings differing in width between a first FET and a second FET, comprising:

forming a first gate stack and a second gate stack overlying a main surface of a substrate;

forming a first spacer on said first and second gate stacks, said first spacer having a vertically extending

portion oriented in a direction generally perpendicular to said main surface, and a horizontally extending portion parallel to said main surface;
forming source and drain regions of said first FET aligned to said first spacer of said first gate stack;
removing said horizontally extending portion of said first spacer by an anisotropic vertical etch process; and
forming source and drain regions of said second FET in said substrate aligned to said vertically extending portion of said first spacer of said second gate stack.

[c16] The method according to claim 15 wherein said first FET is an n-type FET (NFET) and said second FET is a p-type FET (PFET).

[c17] The method according to claim 16 wherein said gate stacks of said first and second FETs are aligned end-to-end in a horizontal direction over said substrate.

[c18] The method according to claim 16 further comprising forming a self-aligned silicide aligned to said source and drain regions of said NFET and said PFET.

[c19] The method according to claim 18 further comprising forming a self-aligned silicide aligned to said gate stacks of said NFET and said PFET.

[c20] An integrated circuit, comprising:

a first field effect transistor (FET) and a second FET, said first FET having source and drain regions each spaced a first distance from a first gate stack of said first FET, said second FET having source and drain regions each spaced a second distance from a second gate stack of said second FET, wherein said first and second distances differ by the width of a horizontally extending portion of a spacer disposed on a sidewall of one of said first and second gate stacks.